

ELASTOMER-SUPPORTED COLD WELDING FOR ROOM TEMPERATURE WAFER-LEVEL BONDING

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ABSTRACT

This paper presents a method for room-temperature wafer-level bonding that is applicable for the MEMS and NEMS packaging and fabrication processes, but does not require an applied voltage, high pressure or vacuum. By applying a layer of elastomer between the wafer and gold overlayer, we successfully bonded two silicon wafers under limited load (~3KPa) at room temperature (25°C).

One of the important potential applications of this technique is to create a temporary cap wafer that would protect already released, bulk or surface-micromachined structures during the dicing process. The initial results of experiments on the detachment of the temporary cap wafers bonded using this method are presented.

1. INTRODUCTION

A number of cold-welding approaches in the MEMS field have been previously reported [1], [2], but the pressure required for most of those methods is in the order of MPa. Another study, however, demonstrated the bonding of metal (gold) surfaces under ambient laboratory conditions without heavy applied loads using elastomeric polydimethylsiloxane (PDMS) supports [3]. The elasticity and compliance of PDMS allow gold surfaces to conform to one another, increasing the area of gold-gold contact and tangentially displacing loosely adsorbed contaminants. Compared with other bonding methods, such as adhesive bonding [4], [5], anodic bonding, eutectic bonding [6], thermocompression bonding [7], and direct bonding [8], this new bonding technique provides strong bonds without requiring any applied voltage, high pressure, elevated temperature or high vacuum. This bonding technique potentially has a range of various applications in the MEMS world, including the fabrication of devices with very restricted thermal budget, packaging, and temporary protection of the devices during the dicing process.

A schematic illustration of the bonding structure is shown in Fig. 1. It is a sandwich-type structure consisting of two silicon wafers with PDMS-supported gold layers in between.

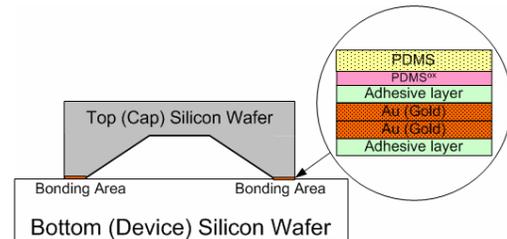


Figure 1: A schematic illustration of the bonding structure

Initial experiments have been performed on silicon wafers, though there are no real limitations on which materials can be bonded using this technique. If the PDMS layers are thick and elastic enough that they enable sufficient conforming of two gold layers, the substrate on which they are deposited is not of paramount importance. However, different substrate materials might need different levels of applied pressure, as our initial experiments have shown.

2. EXPERIMENTAL PROCEDURE

Fig. 2 describes the fabrication process for the top (cap) wafer. The top wafer was a 3-inch silicon wafer, polished on both sides, with a thickness of 375 μ m. First, the dicing map and alignment marks were patterned on one side of the wafer using plasma etching as shown in Fig. 2 (a). The etch was not deep (~90 nm), so that the wafer did not become fragile, and dicing pattern was still visible during the dicing process. Then, LPCVD stoichiometric nitride was deposited on the wafer in preparation for potassium hydroxide (KOH) etching as shown in Fig. 2 (b). A double-side aligner (Research Devices) implemented the front-to-back alignment using the previously etched alignment marks. The pattern on the other side of the wafer is currently a set of bonding test structures of different shapes, sizes and orientations; later on it would be the frame structure corresponding to the locations of the devices on the bottom wafer. After the formation of bonding areas (islands) using KOH etching, the PDMS (Dow Corning Sylgard 184 silicone elastomer) was spin-coated onto the substrate as shown in Fig. 2 (c). The PDMS layer was

patterned using a standard photolithography process [9]. The PDMS was then treated with an oxygen-plasma to increase adhesion to a metal overlayer [10]. Thus, a silica-like layer, PDMS^{ox}, was formed as shown in Fig. 2 (d). Finally, 10 nm of titanium as an adhesive layer and a thin layer of gold (20 nm) were deposited via E-beam evaporation (Indel system) as shown in Fig. 2 (e).

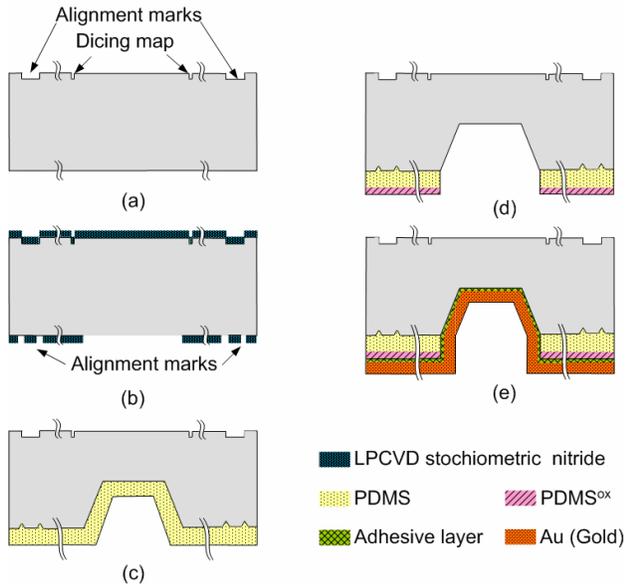


Figure 2: Fabrication process for the top (cap) wafer. (a) Plasma etch the alignment marks and dicing map; (b) Deposit and pattern LPCVD stoichiometric nitride; (c) Spin-coat PDMS on silicon wafer after KOH etch; (d) Plasma etch and oxygen-plasma treat PDMS; (e) E-beam evaporate Ti/Au.

The bottom (device) wafer had only a titanium (10 nm) film and a gold (20 nm) film deposited via E-beam evaporation on top of a RCA-cleaned silicon wafer. In our packaging and temporary encapsulation studies, the bottom wafer will have released surface or bulk micromachined devices.

The method used for performing accurate top-to-bottom alignment that assured the correct position of the encapsulated devices was the customized bonding tool shown in Fig. 3. First, the bonding pairs were put on the stages. One of the stages had a 3-inch round cavity and the other had a corresponding convex shape. The primary flats of wafers were aligned to the alignment poles and corresponding holes on the two stages respectively. Then, the tool was closed together. Additional load (besides 100 g already introduced by putting the wafer stack into this tight enclosure) was added on top of this tool, up to the desired load.

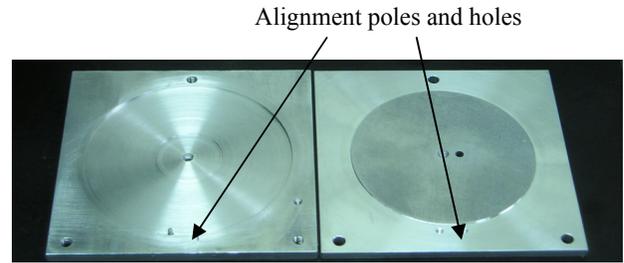


Figure 3: Customized bonding tool

3. RESULTS AND DISCUSSION

PDMS Thickness vs. Spin Speed

Since PDMS is not a standard MEMS material, and its performance can vary depending on the manufacturer supplying it, we have first performed a brief study on the appropriate methods for the PDMS thickness measurement, as well as the dependence of its thickness on the spinning speed and its physical properties.

We have measured the PDMS thickness using three different methods: 1) by positioning the sample on optical microscope using a specially constructed fixture, so that its edge is perpendicular to the eyepiece, and applying the microscope eyepiece reticle calibration (Nikon Filar Micrometer Eyepiece); 2) by using a profilometer; and 3) by using cross-sectional SEM measurements. Profilometry measurements have been reported in the earlier literature [11]. The different results by those three methods are shown in Table 1. When the stylus of the surface profilometer (Tencor alpha-step 200) touched the polymer surface, a deep indentation was clearly observed. This result explains why the profilometry data show much smaller thickness than other measurement types. From Table 1, cross-sectional SEM data confirmed that the optical measurement tool is preferable. The measurement error when using profilometry was around 40%.

Table 1: Comparison of the PDMS thickness data obtained from the different measurement methods

Sample #	PDMS thickness measured using reticle calibration t_1 [μ m]	PDMS thickness measured using profilometer t_2 [μ m]	PDMS thickness measured using SEM t_3 [μ m]	Error of profilometer measurement $(t_3 - t_2)/t_3$ [%]
1	13.6	8.063	13.627	40.8
2	8.1	4.68	7.627	38.6

The dependence of the PDMS thickness as a function of spin rate during spin-coating is shown in Fig. 4. The polymer thickness, t , is strongly related to spin speed (ω), solution concentration (C), and molecular weight (measured by intrinsic viscosity) (η). The empirical equation is given by [12]:

$$t = \frac{KC^\beta[\eta]^\gamma}{\omega^\alpha} \quad (1)$$

where K is an overall calibration constant, and α , β , γ are exponential factors. A fit to the data using Matlab software gave the following values of K , α , β , γ . $K=6.2661$, $\alpha=0.9450$, $\beta=5.2707$, and $\gamma=6.2051$. The values of C (0.90909), η (4000mPa.s) were fixed. [13]

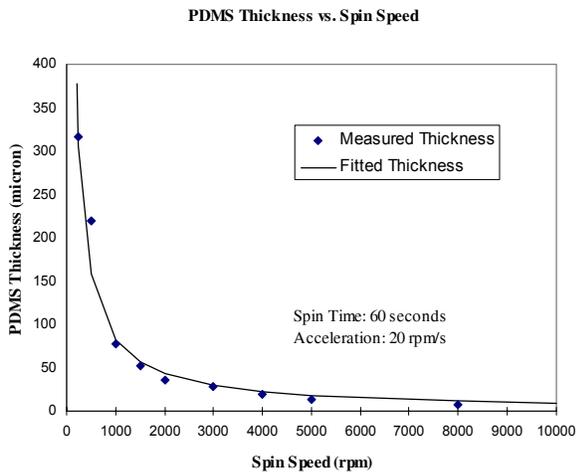


Figure 4: PDMS thickness as a function of spin speed

Adhesive Layer between PDMS & Gold

Experiments have confirmed that the adhesive layer between PDMS and gold was essential in this process. In the case when this layer was not present, delamination of the gold layer occurred during the dicing process. The adhesive layer can be either a self-assembled monolayer (SAM) or a standard material that enhances adhesion like titanium or chromium. A SAM [14] and titanium were chosen for comparison. No huge mechanical strength improvement was made by depositing an SAM layer. In contrast, titanium deposition is convenient because it can be done in the same run as the gold deposition.

Room-Temperature Wafer Bonding

The bonding could be accomplished by simply touching two surfaces prepared in the previously described fashion, without the need for any additional pressure. However, two wafers bonded seamlessly if a small amount of pressure (~3kPa) was applied as shown on Fig. 5. The entire

procedure was performed in a class 100 clean room environment at room temperature (25°C).

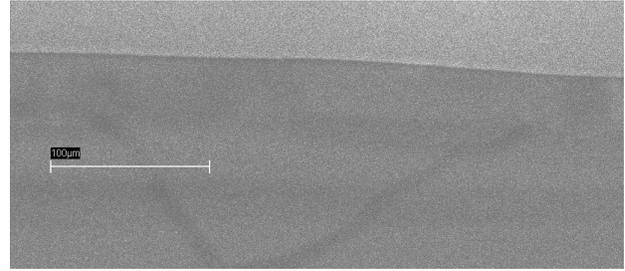


Figure 5: Cross sectional SEM image of bonded interface. Scale bar was 100µm

A key factor that affects the bonding results is the tensile modulus of the PDMS, with a low modulus being preferred for successful bonding. Our results match previous research, which indicated that the polymer tensile modulus will increase as the thickness of the PDMS decreases [15]. Table 2 lists the bonding pressure needed for bonding of test samples which have different thicknesses of PDMS. Those samples are: (1) both dies in the bonding pair have thick (~30 µm) PDMS layers underneath the gold; (2) only one die in bonding pair has a thick (~30 µm) PDMS layer, and the other die has only silicon under the gold; (3) both dies in the bonding pair have thin (~8 µm) PDMS layers under the gold; and (4) only one die in the bonding pair has a thin (~8 µm) PDMS layer, and the other one has only silicon under the gold. The titanium and gold layers were deposited on all the samples using the processing sequence described above. The results reveal that the thinner PDMS layers required greater pressures to bond.

We also successfully bonded a silicon die with a glass die using this method. In this case, PDMS was coated on the silicon die beneath the gold, whereas the glass surface had only gold with an adhesion layer underneath. The applied load to do this bonding was 8.06 KPa and the PDMS thickness was ~30 µm.

Table 2: Relationship between PDMS thickness and minimum load requirement

Sample #	Total PDMS Thickness [µm]	Load required to bond [Pa]
1	~60	≥ 4.29E+01
2	~30	≥ 6.16E+02
3	~16	≥ 1.97E+03
4	~8	≥ 6.57E+04

Detachment of the Temporary Cap Wafer

Initial experiments on the detachment of the bonded cap wafer have been performed. After bonding, the device locations became invisible, so the patterned dicing map was used to guide the dicing saw. After dicing, CF_4/O_2 plasma etching (gas ratio 5:1, 300W, 300mTorr, 15 minutes) was sufficient to remove the PDMS layer at the bonding area. The width of the bonding was 50 μm ; therefore, the cap wafer was detached easily. Currently, we are performing further experiments on the detachment of the cap without damaging the structures underneath (that could happen when the removal is done using plasma processing). Also, we are attempting to form gold enclosures over the devices by complete removal of the PDMS from the cap area.

4. SUMMARY

A new room-temperature wafer-bonding technique has been presented. By adding an elastomeric PDMS support layer beneath the metal (gold) surfaces, wafers bonded at room temperature, and with low applied pressure of only ~3kPa, showed seamless interfaces. Because of the elasticity and compliance of PDMS, gold surfaces conform to one another. Therefore, the area of gold-gold contact is increased and adsorbed contaminants are displaced tangentially.

The tensile modulus of PDMS plays an important role in the bonding result, as expected. The PDMS thickness has been well controlled. An adhesive layer is required between PDMS and metal (gold) layers to complete the dicing process that follows. The comparison of two different choices, a SAM and titanium, has been performed. The titanium layer is preferred because the deposition processing is easier and more compatible to MEMS / IC processing lab without affecting the bonding strength. The initial experiments on the bond-strength characterization as a function of different processing parameters are underway.

Also, successful detaching of the cap and device wafers has been demonstrated, which potentially could have a significant impact for the temporary encapsulation and protection of already released devices during the dicing process. The current detachment process utilizes plasma etching, but alternative processes that are less harmful for the working devices are being explored.

5. ACKNOWLEDGEMENTS

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